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New Process Scheme for Wafer Thinning and Stress-free Separation of Ultra Thin ICs

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Abstract

A new process scheme is proposed that allows manufacturing of 20 μm thin fully processed wafers. Secure handling is achieved by means of carrier substrates using reversible adhesive tapes for connection of support and device wafers. Well established backgrinding and etching techniques are used for wafer thinning. To avoid mechanical damage of thin ICs the "Dicing-by-Thinning" (DbyT) concept is introduced to process flow. Best results are obtained when preparing dry etched chip grooves at front side of device wafer and opening these trenches during backside thinning. The new process scheme was also applied to wafers with highly topographic surfaces. Results of 40 μm thin wafers with 15 μm high Nickel bumps are presented. The "DbyT"-concept is supposed to be a technological basis for an economical manufacturing process for new ultra thin microelectronic products like "Smart Labels".

1. Introduction

During the last years technology for wafer thinning has become a key element for manufacturing of thin semiconductor products like power devices or ICs for smart card applications /ref. 1/. Until today the chip thickness of the IC's is limited to the range of 100 to 200 μm . Completely new applications appear when wafer thinning, dicing and die mounting technology is extended to ultra thin chips with a remaining thickness of 10 - 30 μm . In this range silicon substrates become mechanical flexible and new products like laminate mounted Smart Labels become reality /2/.

Additional impact for the development of thin chip technology arises from present-day packaging requirements. In this context ultra thin IC means maximum miniaturisation and new chances for system integration /3/.

Realisation of advanced integration techniques request cost effective thinning technologies including both stress-free separation of 10 - 30 μm thin wafers and handling concepts for ultra thin dies.

2. Current technology for wafer thinning

Wafer thinning is performed after processing of circuit layers by means of backgrinding equipment. To protect circuit layers a polymeric adhesive tape is laminated to front of wafer. In a first grinding step material is removed by rotating

abrasive wheels containing embedded diamonds, at a rate of 200 - 300 μm per minute. Subsequent fine grinding is performed at lower rates (1 – 10 $\mu\text{m}/\text{min}$) using a polishing wheel that delivers a quite smooth surface. Today's grinding equipment produce wafers with a homogenous thickness: total thickness variation (TTV) is in the range between 0.5 and 2 μm for 150 mm wafers. Grinding leaves a backside damage that extends 5 – 15 μm deep into the substrate.

For thin wafer applications backside damage enhances the risk of wafer breakage. Therefore crystallographic distorted layers are most often removed by a wet-chemical etching process, e. g. spin-etching using isotropic silicon etchant ($\text{HNO}_3/\text{HF}/\text{H}_3\text{PO}_4$). Removal rate for this stress relief process can be chosen between 5 and 40 $\mu\text{m}/\text{min}$; thickness homogeneity is 5 – 10 % of etch removal.

Today backgrinding and spin-etching are standard techniques for wafer thinning [4]. Below a remaining thickness of 150 μm for wafers with diameter of 150 mm specific adaptations for the handling equipment are required. Problems become serious when target thickness should reach values below 100 μm . This has the following reasons: device wafers protected by a tape may be bent by several millimetres due to asymmetrical stress. This prevents usage of cassette handling systems implemented in standard robot equipment. Second reason is a dramatic increase of risk for wafer breakage. As a fully processed wafer may represent a value of some thousands US Dollars wafer breakage is absolutely not acceptable.

3. New process scheme for wafer thinning and die separation

3.1 Reversible mounting technique using adhesive tapes

First aim of this research work was to find a reversible carrier technique that guarantees for secure wafer handling during thinning down to a wafer thickness of 20 μm . When using double side coated adhesive tapes advantages of standard low cost laminating techniques can be combined with benefits of carrier substrates. There are two possibilities for reversible adhesive tapes: UV curable coatings and temperature releasable coatings. Application of UV tapes in combination with carrier substrates require expensive quartz glass support wafers. Therefore focus of experiments was on developing a temperature releasable mounting technique.

Commercially available temperature release tapes are coated with two different polymeric adhesives: one heat-peelable side and one permanently adhesive side. Tapes are laminated onto carrier substrates and cut along wafer edge. Mounting of carrier and device wafer is best performed under vacuum conditions by means of wafer bonding equipment. Vacuum is obligatory to avoid trapping of air bubbles between the two wafers. Air bubbles would cause cracks during grinding of the stacked wafer pair.

Temperature releasable tapes are available for different peel-off temperatures in the range of 90 – 150 $^{\circ}\text{C}$. Therefore it is possible to handle over a wafer from one carrier to another without losing secure support for fragile thin wafers. So you can choose whether wafer front or backside is finally visible on top.

As already mentioned before the desired manufacturing concept for a new thin wafer technology must include a concept for wafer dicing. Actually this requirement plays

an important role, when extremely thin wafers have to be prepared. Mechanical damage at the chip edge induced by a standard wafer saw reveals high risk for chip breakage during back-end chip processing. To overcome this problem the Dicing-by-Thinning concept was developed.

3.2 Dicing-by-Thinning concept

Instead of sawing thin wafers dicing grooves are prepared at wafer front side. Trench depth corresponds to the projected wafer thickness. Preparation of these chip grooves can be accomplished by means of a wafer saw or by silicon dry etching. After mounting the trenched device wafer to the carrier substrate the wafer pair is thinned from its backside until the chip grooves are opened. If chip separation takes place during backside spin-etching, the grooves are rounded by the etchant and possible residual micro-cracks are removed. However it's recommended to stop the process quickly. Otherwise the etchant might penetrate to the wafer front and attack aluminium contact pads. The following micrographs demonstrate the advantage of Dicing-by-Thinning concept. Fig. 1 shows the result after dicing a 30 μm thin wafer by means of a wafer saw: cracks along the cutting line represent a high risk for the mechanical stability of thin ICs.



Fig. 1: Micro-cracks along dicing line after sawing a 30 μm thin wafer.

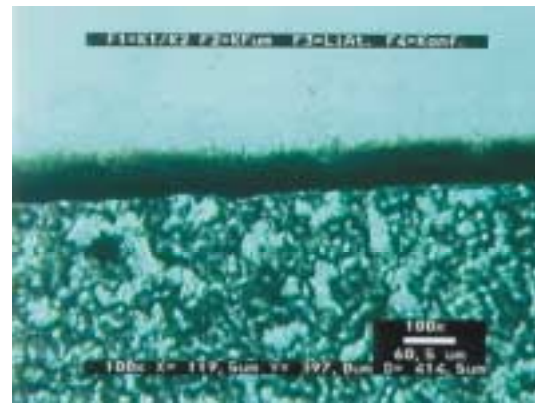


Fig. 2: Smooth dicing line according to the „Dicing-by-Thinning“ concept.

Fig. 2 demonstrates the result according to the Dicing-by-Thinning concept: the side wall of the former chip grooves show smooth edges; no micro cracks are detected. As already mentioned before chip grooves could also be manufactured by dry etching methods. This leads to very interesting new aspects which are described in the next chapter.

3.3 Dicing-by-Thinning using dry etching methods for chip separation

An intended application of extremely thin chips will be mechanical flexible Smart Labels. Such products consist of a very small transponder IC connected to a RF antenna. Die dimensions for the next generation of transponder ICs will be 0.5 x 0.5 mm^2 or smaller. When manufactured on 200 mm wafers, dicing requires several

hours processing time. Even more serious from an economical point of view is the big amount of silicon wafer area that is wasted for cutting lines. Therefore the introduction of dry etching techniques as a future process for die separation is supposed to be a valuable advantage for manufacturing of ultra thin ICs.

Anisotropic dry etching of silicon substrates is well established /5/. For our experiments we used an STS (Surface Technology Systems) equipment. In this work standard photoresist and contact lithography is used to fabricate the desired groove pattern. Resist layer works as a mask for subsequent anisotropic plasma etching by SF_6 gas. Trench width was varied between 5 μm and 100 μm ; trench depth was 30 μm . Etching rates between 2 and 3 $\mu\text{m}/\text{min}$ can be achieved.

As we use a photolithographic pattern groove geometry is no longer restricted to rectangular shapes. As shown in Fig. 3 and 4 hexagonal chip forms or rounded chip corners can be manufactured. Rounded chip shapes may have important benefits for high voltage applications and also for enhanced mechanical reliability during bending.

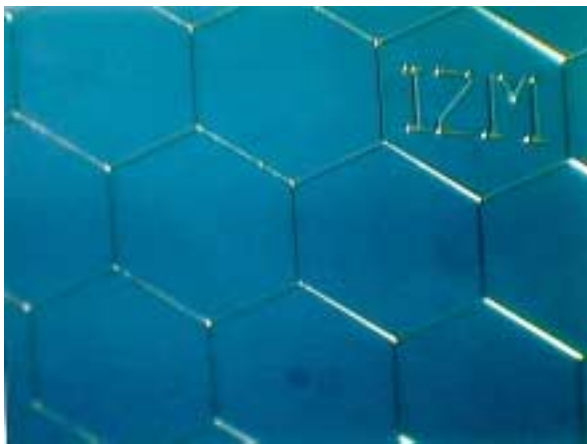


Fig. 3: Hexagonal, 25 μm thin chips; dicing lines are prepared by anisotropic dry etching.

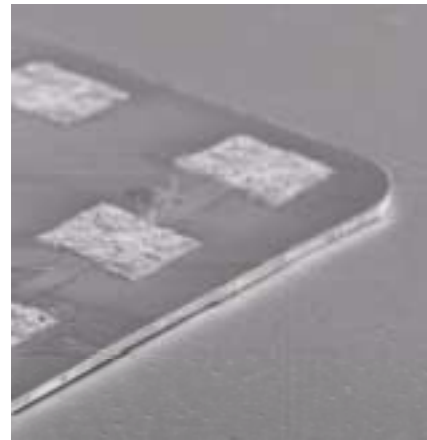


Fig. 4: 25 μm thin single chip with rounded chip corners.

Applying dry etching methods for preparation of chip grooves results in perfectly smooth die edges. Furthermore a big economical advantage can be derived: reducing the geometry of dicing lines from 100 μm to 5 μm and considering a chip geometry of 0.5 mm x 0.5 mm 40 % more ICs can be placed on a wafer.

Crystalline quality of chip edges has a dominant influence to fracture strength of ultra thin ICs. Bending and breaking experiments are just in progress and will be published soon /6/.

4. Thinning of bumped wafers

Grinding of wafers with highly topographic surfaces is a challenging task for thin wafer preparation. This is especially true for wafers with bump metalisation, as it's often used in flip-chip technology. For our experiments we used wafers which have been electroless plated with 15 μm high nickel bumps.

For first experiments the same wafer carrier and mounting technique was used as described in chapter 3.1. After backgrinding to a remaining thickness of 70 μm more than 50 % of test wafers were broken. Obviously adhesive tape could not sufficiently embed surface topography.

So the aim was to find an reversible adhesive tape that could neutralize surface topography, guarantees for a tight connection to carrier substrate during backgrinding and still allows removing of single dies after thinning procedure. Combination of these properties was achieved by laminating two tapes: first a temperature release tape and second a soft UV-curable tape for embedding the bump topography. Process flow has to be modified slightly and is shown and described in the next chapter.

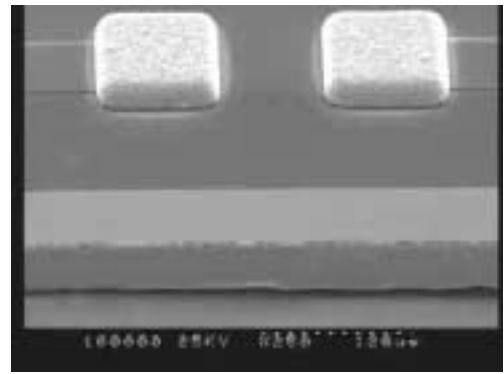


Fig. 5: SEM picture of a 40 μm thin chip with 15 μm high Nickel bumps.

5. Process flow: “DbyT” for wafers with topographic surfaces

- 1) Preparing chip grooves at front side of device wafer by dry etching method (or pre-cutting with wafer saw). Trench depth corresponds to prospected final IC thickness (fig. 6a).
- 2) Laminating low-temperature release tape (T1) to carrier substrate: permanently adhesive side to carrier wafer (fig. 6b).
- 3) Laminating “bump-tape” (T2): UV-curable coating upside (fig. 6b).
- 4) Mounting of carrier and device wafer: connect wafer under vacuum conditions, surface of device wafer upside down (fig. 6c).
- 5) Thinning procedure: grinding down to a remaining thickness of 50 – 70 μm of device wafer, stress-relief etching (i. g. wet-chemical spin-etching) until front side grooves are opened from the backside (fig. 6d).
- 6) Mounting of a second support carrier (wafer or frame-carrier) using a high-temperature release tape.

Fig. 6a)



Fig.6c)

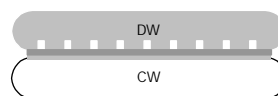


Fig. 6e)

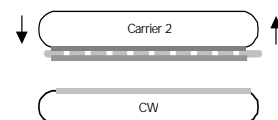


Fig. 6b)

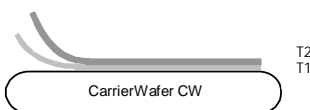


Fig. 6d)

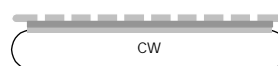


Fig. 6f)

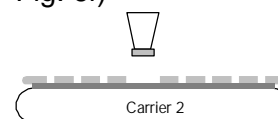


Fig. 6: Handling scheme as proposed by the „Dicing-by-Thinning“ concept; explanations see 5.

- 7) Heating wafer stack to lower release temperature; remove first carrier (fig. 6e).
- 8) UV curing and peel-off "bump-tape"; now you have single ICs mounted front side up on a temperature release tape on a support wafer.
- 9) Continue with die pick-up for IC mounting: pick-up is achieved after a short heating impulse by means of a vacuum tool (fig. 6f).

The concept might be improved in the future at two points of process flow: First is the application of isotropic silicon dry etching as final step for backside thinning and thereby eliminating the risk of IC damage by wet-chemicals at the point of time when the front grooves are opened during backside thinning. Second will be the combination of the two different tapes into one sandwich tape with combined properties. This would be an interesting task for tape manufacturers.

6. Summary

The proposed process scheme "Dicing-by-Thinning" together with the application of dry etching techniques offer a new approach for separation of thin wafers into chips. The process permits manufacturing of ICs with nearly damage free chip edges and allows for non rectangular chip shapes or chips with rounded corners. Specially for small die sizes a large amount of wafer area can be saved.

According to the needs of a manufacturing process a cost effective wafer carrier technique using temperature releasable adhesive tapes was developed. Introducing support wafers to process flow results in distinct advantages for thin wafer handling: practical no risk for wafer breakage, no need for expensive equipment modifications and the capability to extend proven process technologies to larger wafer diameters.

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