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COVER ARTICLE

Addressing Cu contamination via spin-etch cleaning

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While a wafer backside and back edge can be hermetically sealed and protected from copper contamination during electroplating, the front-side exclusion zone and beveled edge are still vulnerable because clamping during electroplating is not a totally effective mask. However, tests have revealed that a proprietary Spin-Process can remove this front-side contamination and any troublesome backside contamination to ≤5 × 10¹⁰ atoms/cm².

The emerging use of copper (Cu) is driving the need for control of any potential Cu cross contamination that could affect yields and fab productivity. Specifically, Cu must be eliminated from a wafer's backside, beveled edge, and front-side edge-exclusion zone so that it is not transmitted to subsequent wafer fabrication operations.

The *1997 National Technology Roadmap for Semiconductors* established target levels for critical metals, including nickel, Cu, and sodium, at $\leq 2.5 \times 10^{10}$ atoms/cm^2 for the 250nm technology node and $\leq 1.3 \times 10^{10}$ atoms/cm^2 for the 180nm node. In other circles, the acceptable level of Cu has not been agreed on; the quoted range is 1×10^{12} atoms/cm^2 to below the 1×10^{10} atoms/cm^2 detection limit of total reflection x-ray fluorescence spectroscopy (TXRF).

The wafer backside has long been a troublesome, ignored source of yield loss. First, metrology tools are not available to measure backside contamination without wafer handling, putting the device side at risk. With Cu processing, aggressive etching solutions are required to remove Cu contamination from the wafer backside. Traditional methods (i.e., wet benches, spray processors, and scrubbers) are not friendly to front-side Cu. With full-coverage Cu, seed and blanket layers readily extend into the exclusion zone and onto the wafer's beveled edge [1]. The wafer backside can be hermetically sealed during Cu deposition, but this leaves the beveled edge and front-side exclusion zone exposed to Cu contamination.

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The Cu fab

Isolating Cu production from the rest of a wafer fab's manufacturing area is one approach that addresses concerns about Cu contamination. But many wafer fabs do not possess a complete set of tools dedicated exclusively to Cu-based, full-flow device processing. So, critical, sophisticated tools such as those for metrology and lithography must accept Cu-processed wafers and ensure that no contamination transfers to non-Cu wafers. Processes and procedures must be developed to control such cross-contamination while also controlling cycle time and cost.

The industry appears to have settled on electroplate deposition for blanket Cu plating of wafers. This process uses backside hermetic sealing and exclusion-zone clamp rings to provide electrical contact and to mask the wafer's exclusion zone from Cu deposition. Energy-dispersive-spectrometry (EDS) data, however, indicate that these rings are not 100% effective in preventing Cu deposition in the exclusion zone (Fig. 1). This condition is further exacerbated by current trends that minimize the exclusion zone to 3mm and even 2mm (as specified by different semiconductor manufacturers), effectively putting the deposited Cu blanket onto the beveled edge.

Clearly, with full-coverage Cu deposition, post-deposition wafers have a Cu film across the front side of the wafer that extends onto the beveled edge and even onto the wafer backside (Fig. 2a). As processing continues, the "ideal" is to remove all excess Cu from the backside around to and including the front-side exclusion zone (Fig. 2b). Failure to achieve the condition depicted in Fig. 2b can result in cross-contamination and subsequent processing problems. For example, Cu in the exclusion zone and on the beveled edge of the wafer can be transferred to cassettes and onto wafer-handling mechanisms in subsequent processes that may also be used for non-Cu wafers. (To combat this concern, SEMATECH used to have "copper Fridays" — Cu wafers were processed through lithography and other steps only on Fridays.

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After this processing, all equipment was decontaminated and non-copper wafers were processed as usual. Now SEMATECH has a "copper anytime" procedure as long as wafers have been processed with the etch cleaning discussed in this article.)

Any Cu contamination is driven into barrier films or silicon on the beveled edge and backside during Cu annealing. Such contamination can be removed after the anneal, but additional sacrificial film is consumed during what amounts to an elongated cleaning process sequence that depends on the sacrificial backside film used, or lack thereof, and depth of Cu diffusion. With only silicon, the process becomes much more complicated; Cu can be eliminated, but the overall cost of processing increases and the thinning of the wafer may not be acceptable.

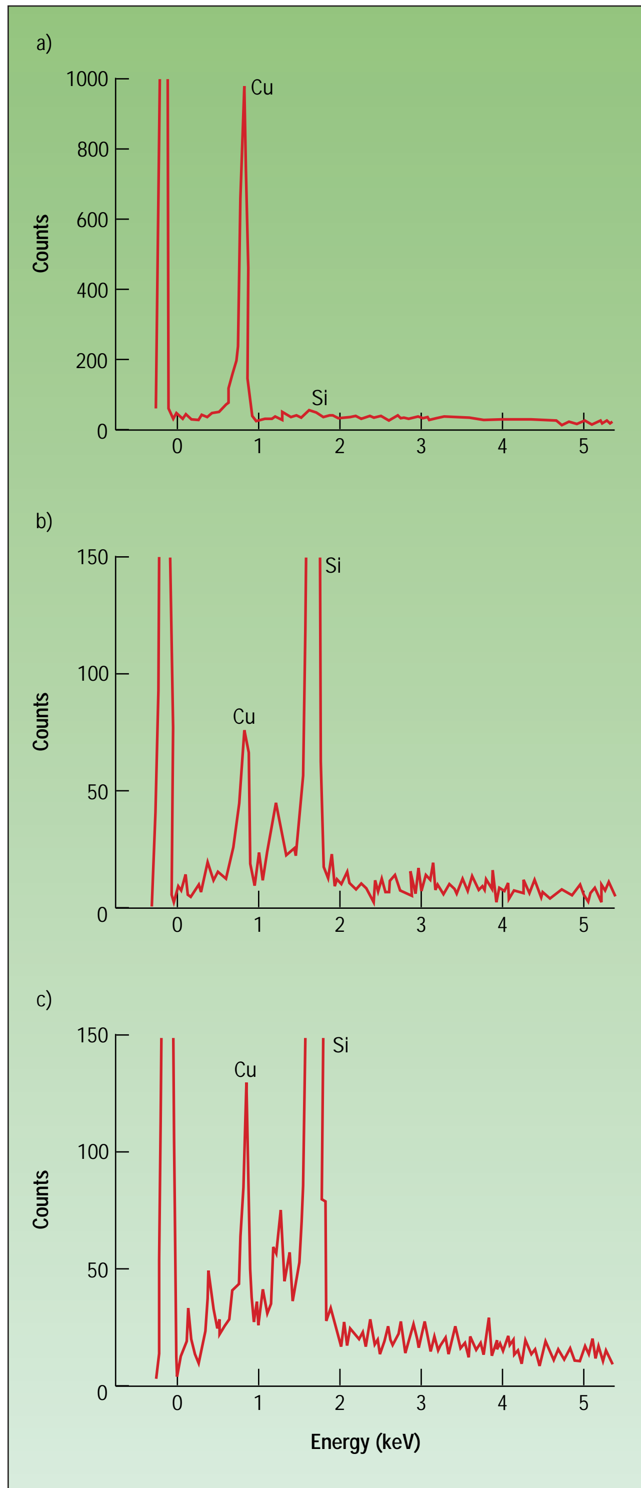


Figure 1. EDS Cu counts after electrochemical deposition of the metal while using a clamp ring; a) 5mm from the wafer edge, b) 3mm, and c) 1mm. (Source: ERSO Taiwan)

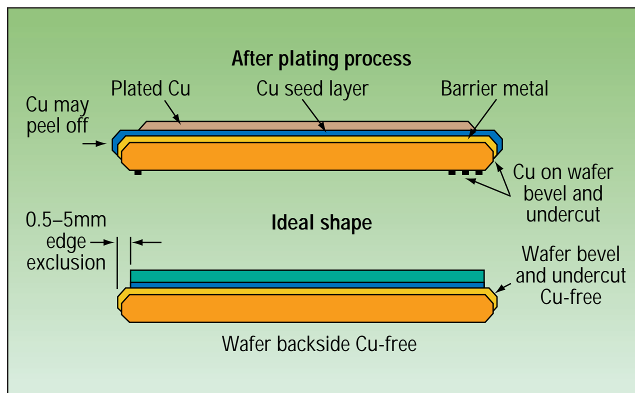


Figure 2. Full-coverage electrochemical Cu plating and the ideal condition after SPCE.

Spin etching

At SEMATECH, recent cooperation between SEZ and major suppliers of Cu deposition equipment has focused on the testing and optimization of Spin-Process contamination elimination (SPCE), a proprietary technology of the SEZ Group. SPCE is a single-wafer processing technology that dispenses a liquid chemical etchant onto the backside of a spinning wafer held front-side-down by a nitrogen cushion and centered with perimeter pins in a Bernoulli wafer chuck. The etchant is dispensed from a radially oscillating overhead nozzle. Control of etchant viscosity, simultaneous radial and tangential etchant flows, and Bernoulli gas flow enables etching of Cu contamination from a wafer backside, and a "wraparound" effect that removes thin-film contamination from the beveled edge and front-side exclusion zone (0.5–5.0mm). (SPCE is also applicable to removing sacrificial oxide, nitride, or other films.)

This work at SEMATECH recognized the lack of methods for detecting Cu on the beveled edge and backside of production wafers. We used vapor phase dissolution inductively coupled plasma mass spectrometry (VPD-ICP-MS or VPD) to measure the beveled edge. Showing that the beveled edge is clean after a process step is difficult, however, and testing methods lead to speculation on the quality of the results, because VPD data are highly dependent on the techniques used during the process. We used TXRF to measure the backside, but this involves placing a wafer front-side-down, precluding use of this method with production wafers. We tested the exclusion zone with EDS.

Our tests have shown that SPCE is effective after a clamp-ring Cu deposition. Data in Fig. 3 show that EDS counts for Cu dropped from the thousands to 30 at 5mm from the edge in the exclusion zone and to below the detection level near the edge of the wafer. (Compare data in Fig. 1 and Fig. 3.)

To ensure effective contamination removal and improved device performance of die at the edge of the wafer, a barrier film will aid in the removal of contamination. The barrier film is key to yield enhancement and overall cost reduction. Current Cu deposition methodologies do not ensure that the Cu film will only be deposited in the device region of the wafer. Therefore, a barrier film is required to ensure the increased profitability that should accompany the introduction of the Cu interconnect.

We determined that a key point to successful use of SPCE is

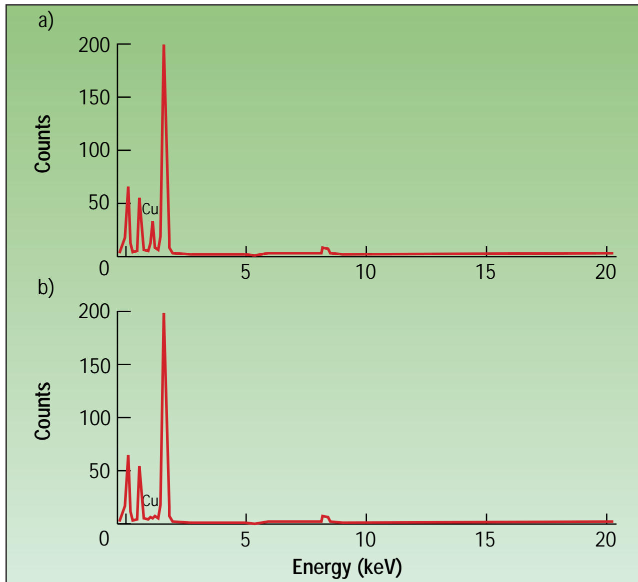


Figure 3. EDS counts for Cu dropped from the thousands to a) 30 at 5mm from the edge in the exclusion zone and to b) below detection level near the edge of the wafer.

the presence of a barrier film. If silicon is left exposed — not covered by tantalum tantalum-nitride, silicon oxide, or another barrier film — Cu readily diffuses into it. Removing Cu after an anneal is more difficult, but not impossible. Ideally, a two-step process is best: 1) Cu removal, and 2) etching off the silicon. The amount of silicon removed depends on the wafer's temperature prior to cleaning; if the wafer is annealed before SPCE, excessive amounts of silicon may have to be removed to remove contamination. TXRF data show that bare silicon wafers exposed to Cu contamination may still have *extreme* amounts of Cu after the cleaning process (see table). But after the second step in the process, the silicon etch, Cu is generally below detection limits.

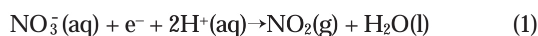
We performed additional testing of the SPCE process to quantify the effectiveness of removing Cu deposited over an oxide film. TXRF results after SPCE showed an average of 1.6×10^{10} Cu atoms/cm^2. VPD results showed 8.3×10^{10} Cu atoms/cm^2.

Removal of Cu films and contamination can be accomplished with a myriad of different solutions [2]. In our tests at SEMATECH, we used a solution of phosphoric, nitric, and sulfuric acids. Nitric acid (HNO_3) is an oxyacid and as such is a strong electrolyte and a powerful oxidizing agent that is considered 100% ionized in aqueous solution (H_2O). The oxidation number (N) of nitrogen in HNO_3 is +5. The most common reduction products of nitric acid are NO_2 (N = 4), NO (N = 2), and NH_4^+ (N = –3).

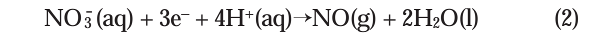
TXRF measurements of Cu after SPCE and subsequent silicon etch

Wafer location (mm, mm)	After Cu strip (10^{10} atoms/cm^2)	After Si etch (10^{10} atoms/cm^2)
0,0	19502	<0.5
40,40	14212	1.8
40,–40	13887	<0.5
–40,40	12230	<0.5
–40,–40	12871	<0.5

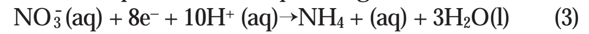
The half-reactions yielding these products are:



$$NO_3^-(aq) + e^- + 2H^+(aq) \rightarrow NO_2(g) + H_2O(l) \quad (1)$$



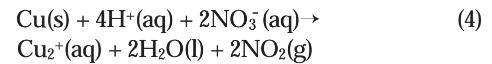
$$NO_3^-(aq) + 3e^- + 4H^+(aq) \rightarrow NO(g) + 2H_2O(l) \quad (2)$$



$$NO_3^-(aq) + 8e^- + 10H^+(aq) \rightarrow NH_4 + (aq) + 3H_2O(l) \quad (3)$$

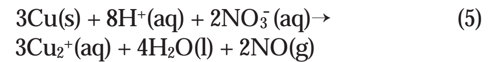
It is rare for one of the reactions to occur to the total exclusion of the other two. Nitric acid will oxidize most metals to the corresponding cations and will oxidize metals both above and below hydrogen in the electromotive series. Since the stronger oxidizing agent in HNO_3 is the NO_3^- ion (not H^+), the reduction product is NO_2, NO, or NH_4^+ (not H_2) [3].

Concentrated nitric acid is an extremely rapid etchant of Ni, while hydrofluoric acid (HF) is relatively slow. Solutions of HF:HNO_3 are relatively fast and more controllable than straight HNO_3 with removal rate reduced by increasing the ratio of HF [2]. The extent to which the reduction of nitric acid takes place is a function of the concentration of the acid, the temperature at which the reaction is carried out, and the nature of the reducing agent. The reaction in Eqn. 1 is predominant when concentrated (70%) nitric acid reacts with Cu [3]:



$$Cu(s) + 4H^+(aq) + 2NO_3^-(aq) \rightarrow Cu_2^+(aq) + 2H_2O(l) + 2NO_2(g) \quad (4)$$

The reaction in Eqn. 2 is predominant when Cu reacts with a mixture of equal volumes of concentrated nitric acid and water:



$$3Cu(s) + 8H^+(aq) + 2NO_3^-(aq) \rightarrow 3Cu_2^+(aq) + 4H_2O(l) + 2NO(g) \quad (5)$$

In the table data, we etch bare silicon with Merck's Spinetch solution to remove the diffused Cu. With a thermal oxide or nitride film present, the second-step film removal is not required and the phosphoric-nitric-sulfuric solution must be adjusted, replacing sulfuric acid with HF acid. Adjusting the HF concentration enables rapid removal of oxide or nitride while the Cu contamination is being reduced.

The Cu fab's future

In general, semiconductor manufacturers adopting Cu processing will conservatively decide that they do not want Cu in the exclusion zone on wafers moving on to anneal after deposition, excluding Cu from perhaps as much as a 5mm perimeter from the front of the wafer. We demonstrated that the SPCE process can remove Cu from the wafer front-side exclusion zone on 200mm wafers, and it is "tunable" from 0.5–5mm.

Failure to remove Cu from the exclusion zone may not be detrimental to the device, since diffusion through tantalum nitride is minimal below 400°C [4]. Theoretically, however, during chemical mechanical planarization (CMP), the exclusion zone would be free of Cu, but serious concerns remain for cross-contamination from the remaining Cu film on the beveled edge. CMP processes can only remove copper from the face of the wafer, leaving any film or contamination on the beveled edge free to migrate during subsequent operations.

Expectations among semiconductor manufacturers that all wafers exiting a Cu process will meet specified contamination limits raises several issues:

- Can deposition and CMP equipment suppliers effectively clean all regions of a wafer as part of an integrated process?
- Do equipment suppliers have the room to integrate such a cleaning system?
- What does this do to the cost of the system?
- What about wafer rework and equipment flexibility?

The answers lie with the users. They all have their own idea of where and how they want Cu systems integrated and to what extent they will sacrifice flexibility. Initially, stand-alone

systems may be the best way to get answers to these questions. This will enable fabs to determine, during a pilot-line phase, where, when, and how often cleans should take place and what contamination level is acceptable. One potential scenario is that standalone systems provide the flexibility and process capability required and the yield results that offset the difficulties of handling Cu-contaminated wafers.

Conclusion

Tests of SPCE processing, which can etch-clean a wafer's backside, front-side beveled edge, and exclusion zone to remove Cu and other films, show that this is a reliable method for eliminating Cu contamination. Remaining contamination after SPCE, measured by TXRF, is regularly $<5 \times 10^{10}$ atoms/cm^2. The qualification of this process' reliability is important to semiconductor manufacturing, in which available contamination-monitoring techniques are not conducive to measuring production wafers without the risk of front-side damage.

Still to be resolved is the removal of Cu processing's tantalum tantalum-nitride film from the exclusion zone. The answer here seems to revolve around whether Cu processes will be required to guarantee Cu contamination levels after a wafer's departure from the equipment.

Can wafer fabrication budgets afford the expenditure of millions of dollars on dedicated Cu production equipment? No matter what the answer, the need for the SPCE process is immediate, critical, and increasing. ■

Acknowledgments

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